

# **Notice of References Cited**

Application No.  
09/069,054

Applicant(s)  
Richard CHAN et al.

Examiner  
A.M. Thompson

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2768

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## **U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	4,758,745 ✓	07/19/88	Elgamal et al.	307	465
B	5,594,367 ✓	01/14/97	Trimberger et al.	326	41
C	5,835,751 ✓	11/10/98	Chen et al.	395	500
D	5,304,860 ✓	04/19/94	Ashby et al.	307	296.3
E	5,338,983 ✓	08/16/94	Agarwala	307	465
F	5,347,181 ✓	09/13/94	Ashby et al.	307	465
G	5,991,908 ✓	11/23/99	Baxter et al.	714	727
H	5,959,466 ✓	09/28/99	McGowan	326	39
I	5,874,834 ✓	02/23/99	New	326	39
J	5,469,003 ✓	11/21/95	Kean	326	39
K	5,452,231 ✓	09/19/95	Butts et al.	364	489
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V	M. Karjalainen et al., Block Diagram Compilation and Graphical Editing of DSP Algorithms in the QuickSig System, IEEE Circuits and Systems, pp. 1057-1060	06/88
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X	A. El Gamal, An Architecture for Electrically Configurable Gate Arrays, IEEE Journal of Solid State Circuits, pp. 394-398	04/89

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